WHAT IS CLAIMED IS:

1. A method for fabricating an integrated circuit comprising the steps of:

fabricating a portion of an integrated circuit comprising at least one active circuit area; and

fabricating a redistribution metal layer in said integrated circuit during a fabrication process of said portion of said integrated circuit.

2. The method as set forth in Claim 1 further comprising the step of:

fabricating portions of said redistribution metal layer that are open to receive a solder bump.

3. The method as set forth in Claim 1 further comprising the steps of:

fabricating an active circuit area and an associated metal pad on a base substrate;

fabricating a vertical plug of a redistribution metal layer;

mounting said vertical plug of said redistribution metal layer on said metal pad;

electrically connecting said vertical plug of said redistribution metal layer to said metal pad;

depositing an undoped silicon oxide layer on said active circuit area and on said metal pad;

depositing a phosphosilicate glass layer on said undoped silicon oxide layer;

depositing a silicon oxynitride layer over said phosphosilicate glass layer;

depositing a flat redistribution metal layer over said silicon oxynitride layer; and

electrically connecting said flat redistribution metal layer to said vertical plug of said redistribution metal layer.

4. The method as set forth in Claim 3 further comprising the steps of:

depositing a polyimide layer over portions of said flat redistribution metal layer and over portions of said silicon oxynitride layer; and

etching portions of said polyimide layer to leave portions of said flat redistribution metal layer open to receive a solder bump.

5. The method as set forth in Claim 1 further comprising the steps of:

fabricating an active circuit area and an associated metal pad on a base substrate;

depositing an undoped silicon oxide layer on said active circuit area and on said metal pad;

depositing a phosphosilicate glass layer on said undoped silicon oxide layer;

depositing a redistribution metal layer over said phosphosilicate glass layer;

electrically connecting said redistribution metal layer to said metal pad; and

depositing a silicon oxynitride layer over portions of said redistribution metal layer.

6. The method as set forth in Claim 5 further comprising the step of:

leaving portions of said redistribution metal layer open to receive a solder bump.

7. The method as set forth in Claim 5 further comprising the step of:

depositing a silicon oxynitride layer over all portions of said redistribution metal layer.

8. The method as set forth in Claim 7 further comprising the step of:

etching said silicon oxynitride layer to a pattern that leaves portions of said redistribution metal layer uncovered to receive a solder bump.

9. The method as set forth in Claim 5 further comprising the steps of:

depositing a polyimide layer over portions of said redistribution metal layer and over portions of said silicon oxynitride layer; and

etching portions of said polyimide layer to leave portions of said flat redistribution metal layer open to receive a solder bump.

10. The method as set forth in Claim 1 further comprising the step of:

fabricating said redistribution metal layer using a last metal layer that is used to fabricate an active circuit area of said integrated circuit.

11. An integrated circuit comprising:

a portion of an integrated circuit comprising at least one active circuit area; and

a redistribution metal layer in said integrated circuit fabricated during a fabrication process of said portion of said integrated circuit.

12. The integrated circuit as set forth in Claim 11 wherein portions of said redistribution metal layer in said integrated circuit are open to receive a solder bump.

13. The integrated circuit as set forth in Claim 11 further comprising:

an active circuit area and an associated metal pad on a base substrate;

a vertical plug of a redistribution metal layer mounted on and electrically connected to said metal pad;

a layer of undoped silicon oxide layer deposited on said active circuit area and on said metal pad;

a phosphosilicate glass layer deposited on said undoped silicon oxide layer;

a silicon oxynitride layer deposited on said phosphosilicate glass layer; and

a flat redistribution metal layer deposited over said silicon oxynitride layer;

wherein said flat redistribution metal layer is electrically connected to said vertical plug of said redistribution metal layer.

14. The integrated circuit as set forth in Claim 13 further comprising:

a polyimide layer deposited over portions of said flat redistribution metal layer and over portions of said silicon oxynitride layer;

wherein said polyimide layer is etched to leave portions of said flat redistribution metal layer open to receive a solder bump.

15. The integrated circuit as set forth in Claim 11 further comprising:

an active circuit area and an associated metal pad on a base substrate;

an undoped silicon oxide layer deposited on said active circuit area and on said metal pad;

a phosphosilicate glass layer deposited on said undoped silicon oxide layer;

a redistribution metal layer deposited over said phosphosilicate glass layer, wherein said redistribution metal layer is electrically connected to said metal pad; and

a silicon oxynitride layer deposited over portions of said redistribution metal layer.

16. The integrated circuit as set forth in Claim 15 wherein portions of said redistribution metal layer are open to receive a solder bump.

17. The integrated circuit as set forth in Claim 15 further comprising:

a silicon oxynitride layer deposited over said redistribution metal layer etched to a pattern that leaves portions of said redistribution metal layer uncovered to receive a solder bump.

18. The integrated circuit as set forth in Claim 15 further comprising:

a polyimide layer deposited over portions of said redistribution metal layer and over portions of said silicon oxynitride layer;

wherein portions of said redistribution metal layer are open to receive a solder bump.

19. The integrated circuit as set forth in Claim 11 further comprising:

a redistribution metal layer fabricated using a last metal layer that is used to fabricate an active circuit area of said integrated circuit.

20. The integrated circuit as set forth in Claim 12 further comprising:

a solder bump attached to said portions of said redistribution metal layer of said integrated circuit that are open to receive a solder bump.

21. The integrated circuit as set forth in Claim 14 further comprising:

a solder bump attached to said portions of said flat redistribution metal layer of said integrated circuit that are open to receive a solder bump.

22. The integrated circuit as set forth in Claim 16 further comprising:

a solder bump attached to said portions of said flat redistribution metal layer of said integrated circuit that are open to receive a solder bump.

23. A method for fabricating an integrated circuit comprising the steps of:

fabricating a first portion of an active circuit area and an associated metal pad on a base substrate, said first portion of said active circuit area comprising a next to last metal layer;

depositing a passivation layer on said first portion of said active circuit area and on said metal pad;

etching at least one via through said passivation layer to said metal pad;

etching a metal layer pattern into said passivation layer;

depositing a last metal layer onto said metal layer pattern on said passivation layer to form a redistribution metal layer; and

depositing said last metal layer onto said first portion of said active circuit area to form a complete active circuit area.

24. The method as claimed in Claim 23 further comprising the step of:

polishing a surface of said redistribution metal layer to produce a flat surface on said redistribution metal layer.

25. The method as claimed in Claim 23 further comprising the step of:

depositing said last metal layer into at least one via to electrically connect said metal pad to said redistribution metal layer.

26. An integrated circuit comprising:

a first portion of an active circuit area and an associated metal pad on a base substrate, said first portion of said active circuit area comprising a next to last metal layer;

a passivation layer deposited on said first portion of said active circuit area and on said metal pad;

at least one via etched through said passivation layer to said metal pad;

a metal layer pattern etched into said passivation layer; and

a redistribution metal layer deposited on said metal layer pattern in said passivation layer, wherein said redistribution metal layer comprises a last metal layer, and wherein a portion of said last metal layer is deposited on said first portion of said active circuit area to form a complete active circuit area.

27. The integrated circuit as claimed in Claim 26 comprising metal within said at least one via, wherein said metal within said at least one via forms a unitary structure with said redistribution metal layer.

28. The integrated circuit as claimed in Claim 27 wherein said metal within said at least one via electrically connects said metal pad to said redistribution metal layer.

29. The integrated circuit as claimed in Claim 26 wherein a surface of said redistribution metal layer deposited on said metal layer pattern in said passivation layer comprises a flat surface open to receive a solder bump.

30. The integrated circuit as claimed in Claim 29 further comprising:

a solder bump attached to said flat surface of said redistribution metal layer open to receive a solder bump.